

Simulation environment

- PDK: Skywater130
- Schematic capture tool: Xschem
- Simulator: Ngspice
- Waveform viewer: Xschem built-in waveform graph
- Test bench: SIM_current_mirror.sch

Current Mirror Mismatch Monte Carlo Test Bench

The image displays a simulation environment for a current mirror circuit. At the top left, a plot shows the drain current $i(vds)$ in microamperes (μA) over time. The y-axis ranges from 950n to 1.1u, and the x-axis shows time points at 460n, 480n, and 500n. The plot shows multiple horizontal lines representing the current for different Monte Carlo runs, indicating a distribution of values around a mean of approximately 1.0uA.

Below the plot is a schematic diagram of a current mirror circuit. It consists of two NMOS transistors, M1 and M2, both of type 'nfet_01v8' with a width-to-length ratio of $1 \times 1/5$. The gates of both transistors are connected to a common gate voltage v_g . The source of M1 is connected to ground (GND), and its drain is connected to the gate of M2. The source of M2 is also connected to GND, and its drain is connected to a load resistor v_1 with a value of 0.9. The drain voltage of M2 is labeled v_d , and the drain current is labeled $i(vds)$. A current source in with a value of 1u is connected to the gate of M1.

To the right of the schematic, there are two green arrows pointing to the right, labeled 'Load waves' and 'Annotate OP'. Below these arrows is a small icon representing a corner file, labeled 'Corner: tt_mm'.

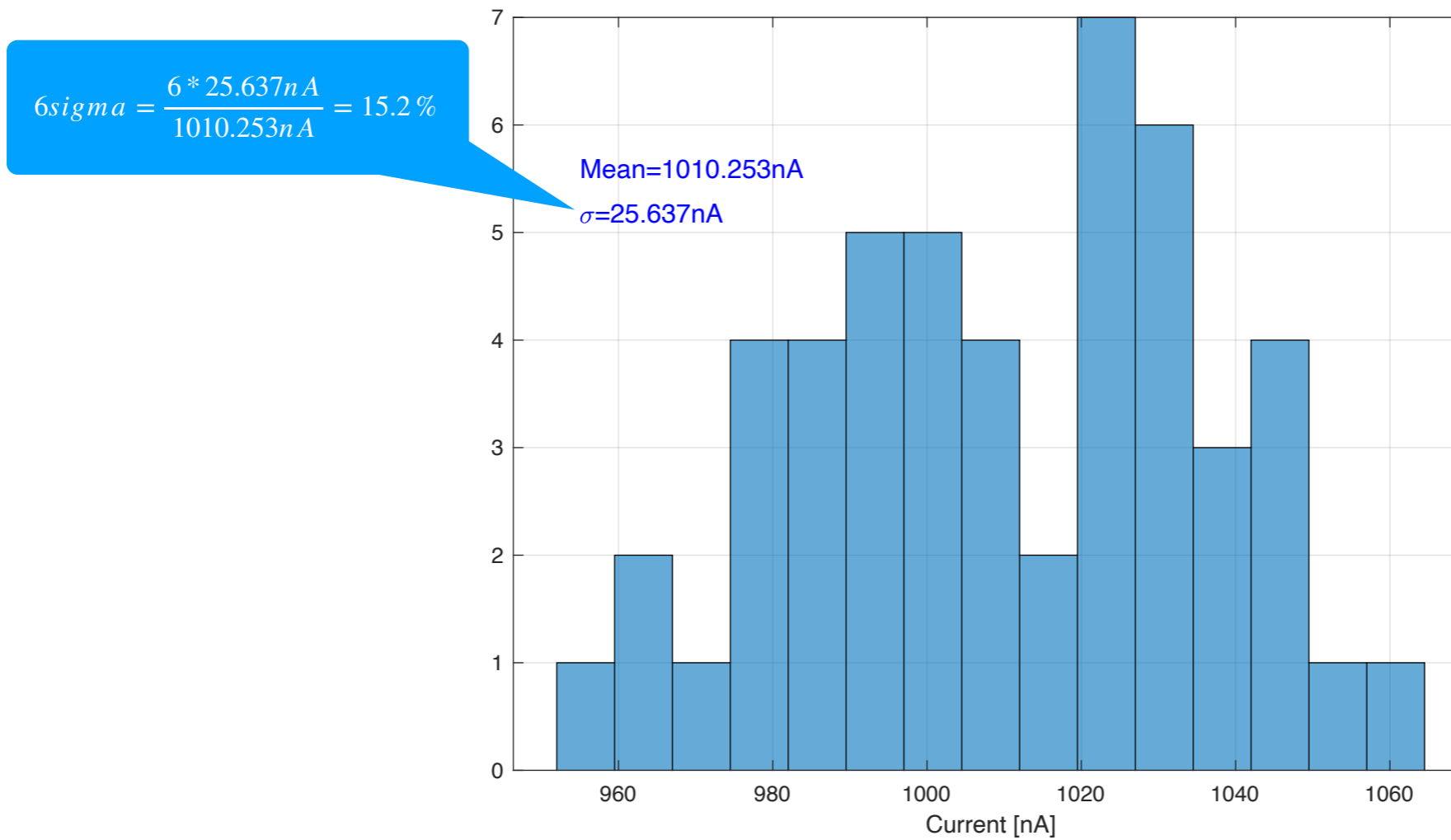
At the bottom left, the 'XSCHM' logo is visible. In the center, the text reads 'Ming Sun' and 'schematic/test/SIM_current_mirror.sch'. At the bottom right, the timestamp '2022-11-12 08:56:53' is displayed.

```
stimulus
.option chgtol=4e-16 method=gear
.param TEMPGAUSS = agauss(40, 30, 1)
.option temp = 'TEMPGAUSS'

.control
option seed = 8
let run = 1
save all
op
write SIM_current_mirror.raw
reset
set appendwrite
dowhile run <= 30
save @m.xml1.msky130_fd_pr_nfet_01v8[gm]
+ @m.xml1.msky130_fd_pr_nfet_01v8[id]
+ @m.xml1.msky130_fd_pr_nfet_01v8[vgs]
+ @m.xml1.msky130_fd_pr_nfet_01v8[cgg]
+ @m.xml1.msky130_fd_pr_nfet_01v8[vds]
+ @m.xml1.msky130_fd_pr_nfet_01v8[vdsat]
+ @m.xml1.msky130_fd_pr_nfet_01v8[vth]
+ @m.xml2.msky130_fd_pr_nfet_01v8[gm]
+ @m.xml2.msky130_fd_pr_nfet_01v8[id]
+ @m.xml2.msky130_fd_pr_nfet_01v8[vgs]
+ @m.xml2.msky130_fd_pr_nfet_01v8[cgg]
+ @m.xml2.msky130_fd_pr_nfet_01v8[vds]
+ @m.xml2.msky130_fd_pr_nfet_01v8[vdsat]
+ @m.xml2.msky130_fd_pr_nfet_01v8[vth]
* save all
tran 1n 1u uic
write SIM_current_mirror.raw
let run = run + 1
reset
end
.endc
```

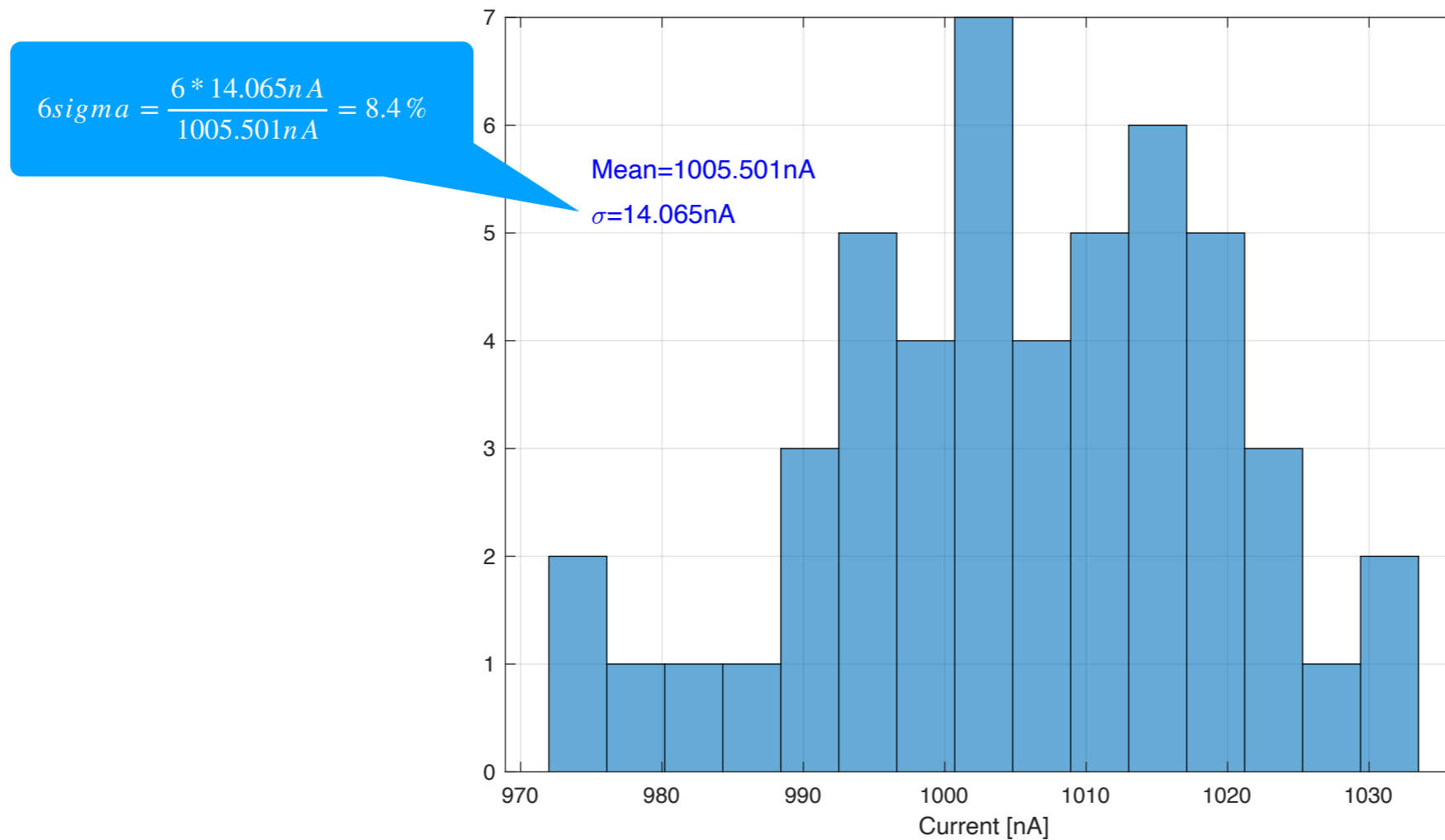
1.8V NMOS Monte Carlo sim result

- $W=1\mu\text{m}$, $L=5\mu\text{m}$



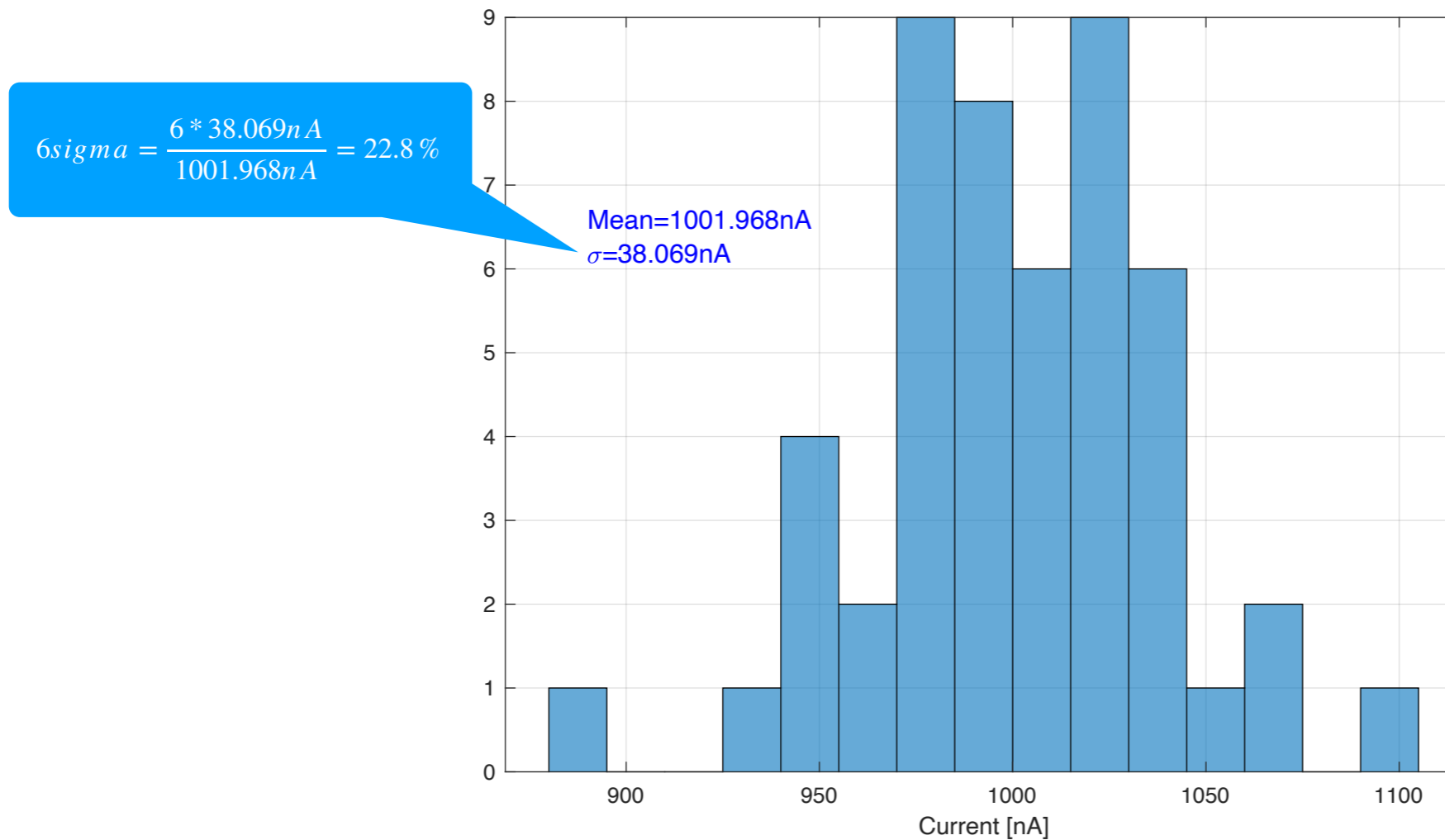
1.8V NMOS Monte Carlo sim result

- $W=2\mu\text{m}$, $L=10\mu\text{m}$ → area 4x, mismatch improves by ~2x



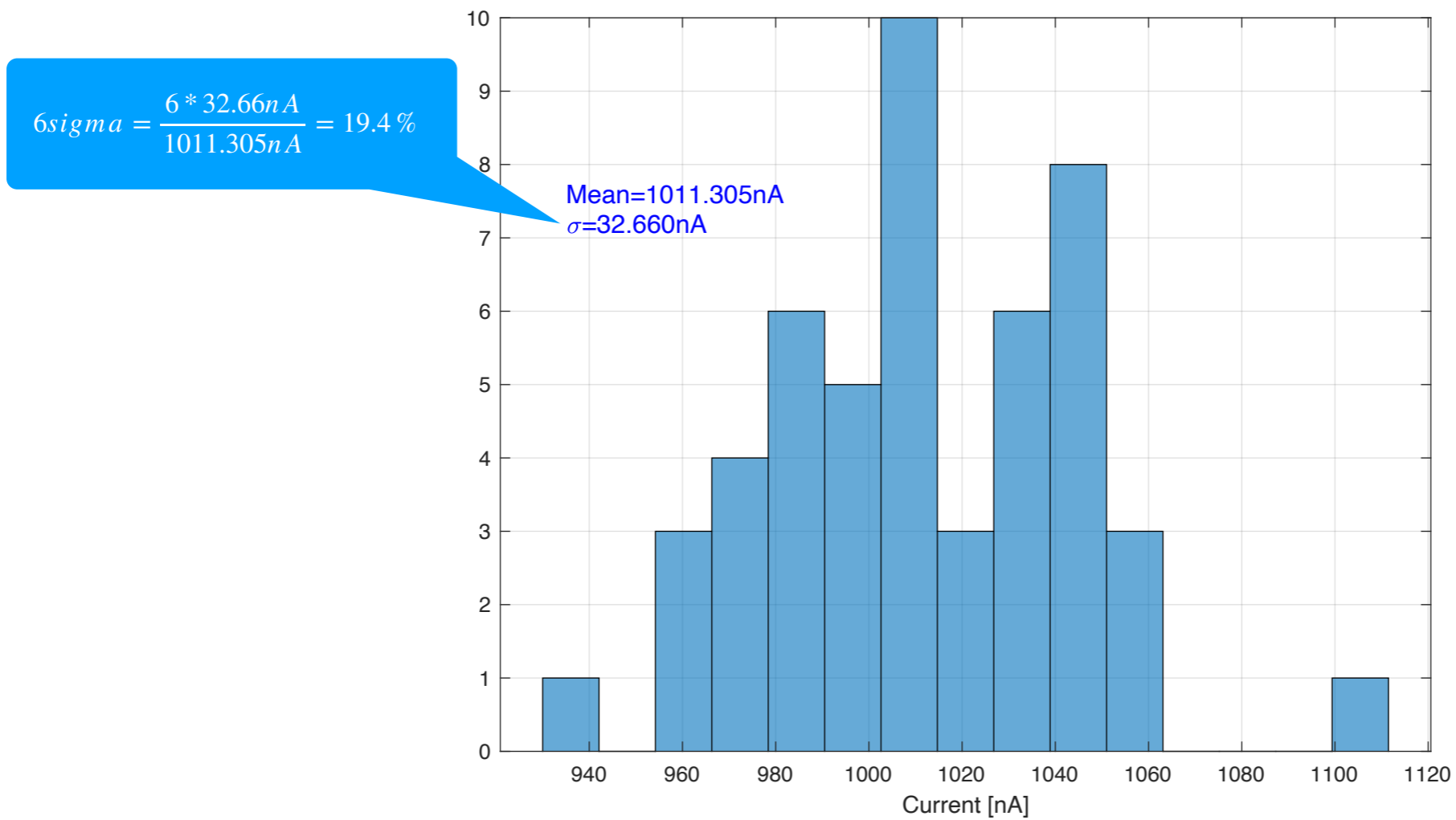
1.8V NMOS Monte Carlo sim result

- $W=0.5\mu\text{m}$, $L=5\mu\text{m}$



1.8V NMOS Monte Carlo sim result

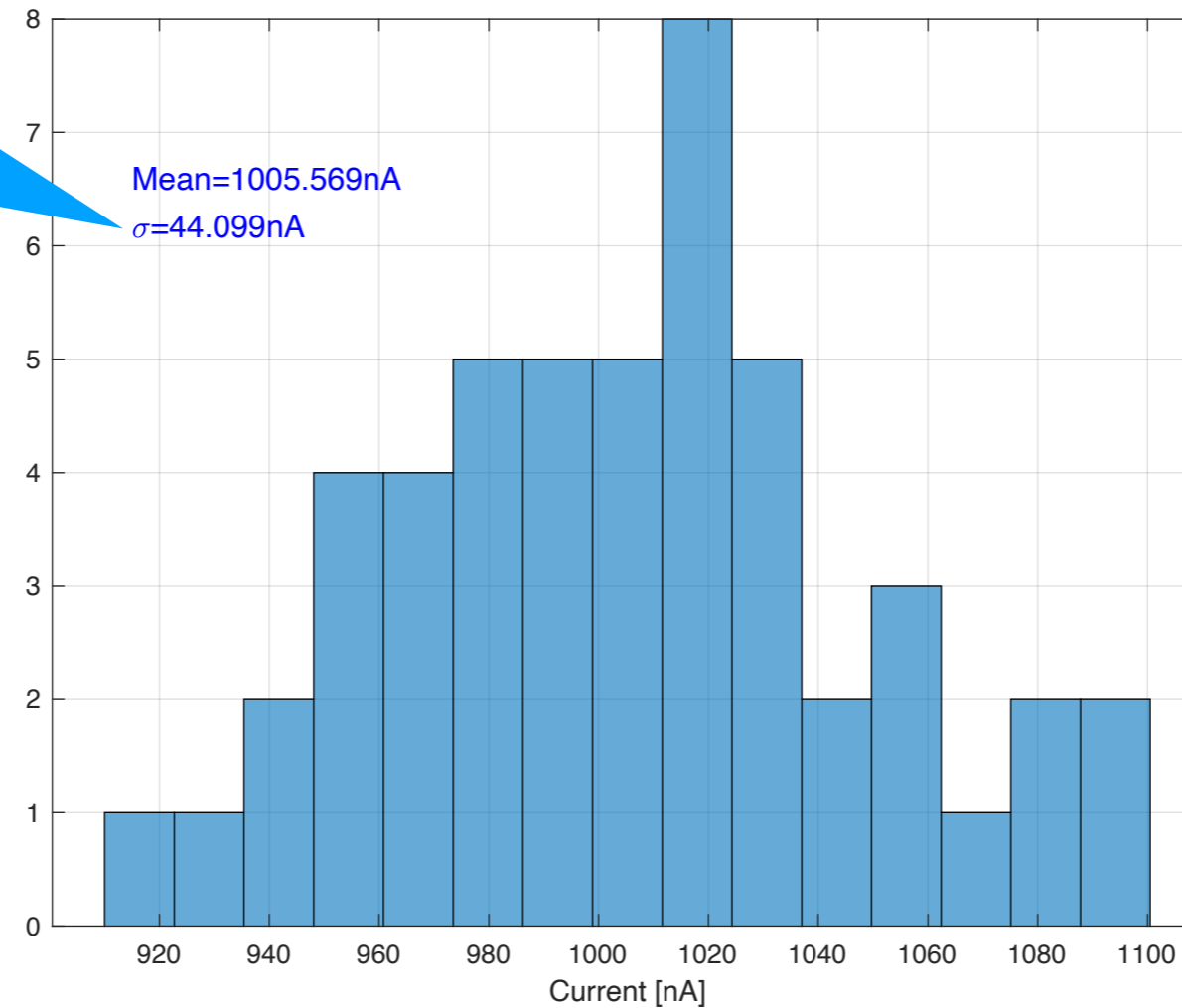
- $W=1\mu\text{m}$, $L=4\mu\text{m}$



1.8V LVT NMOS Monte Carlo sim result

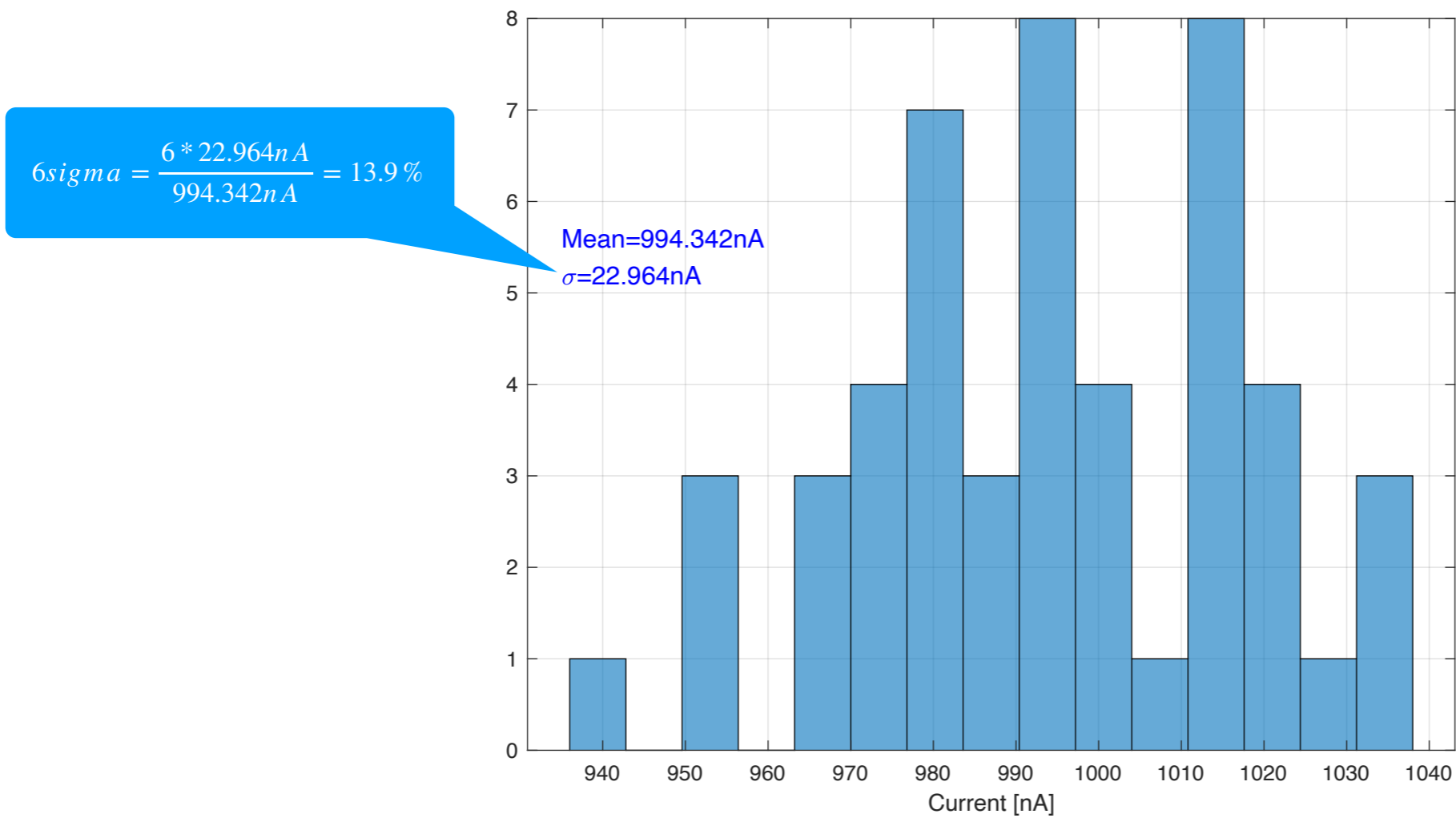
- $W=1\mu\text{m}$, $L=4\mu\text{m}$

$$6\sigma = \frac{6 * 44.099\text{nA}}{1005.569\text{nA}} = 26.3\%$$



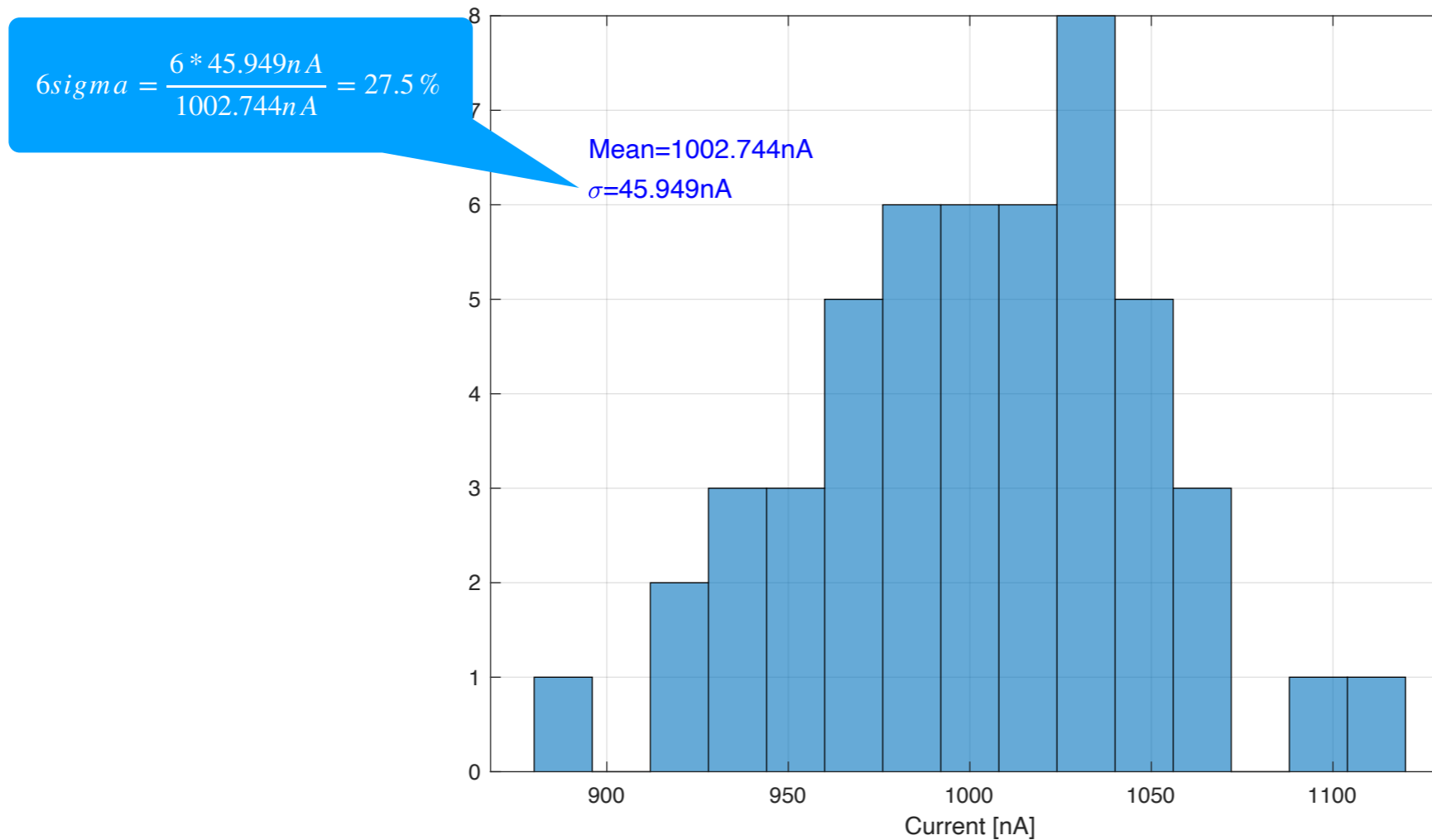
1.8V PMOS Monte Carlo sim result

- $W=1\mu\text{m}$, $L=4\mu\text{m}$



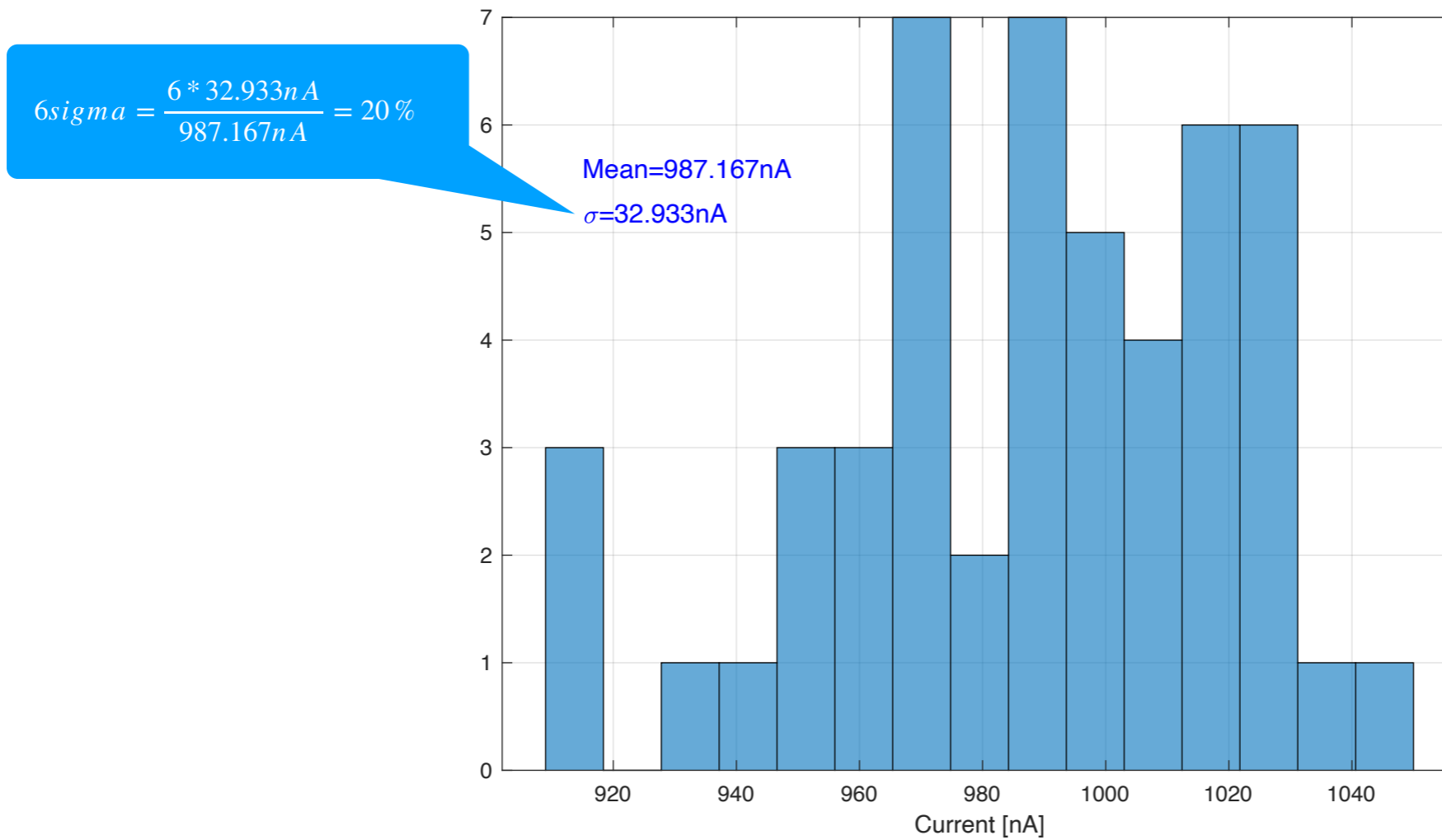
1.8V PMOS Monte Carlo sim result

- $W=2\mu\text{m}, L=2\mu\text{m}$



1.8V PMOS Monte Carlo sim result

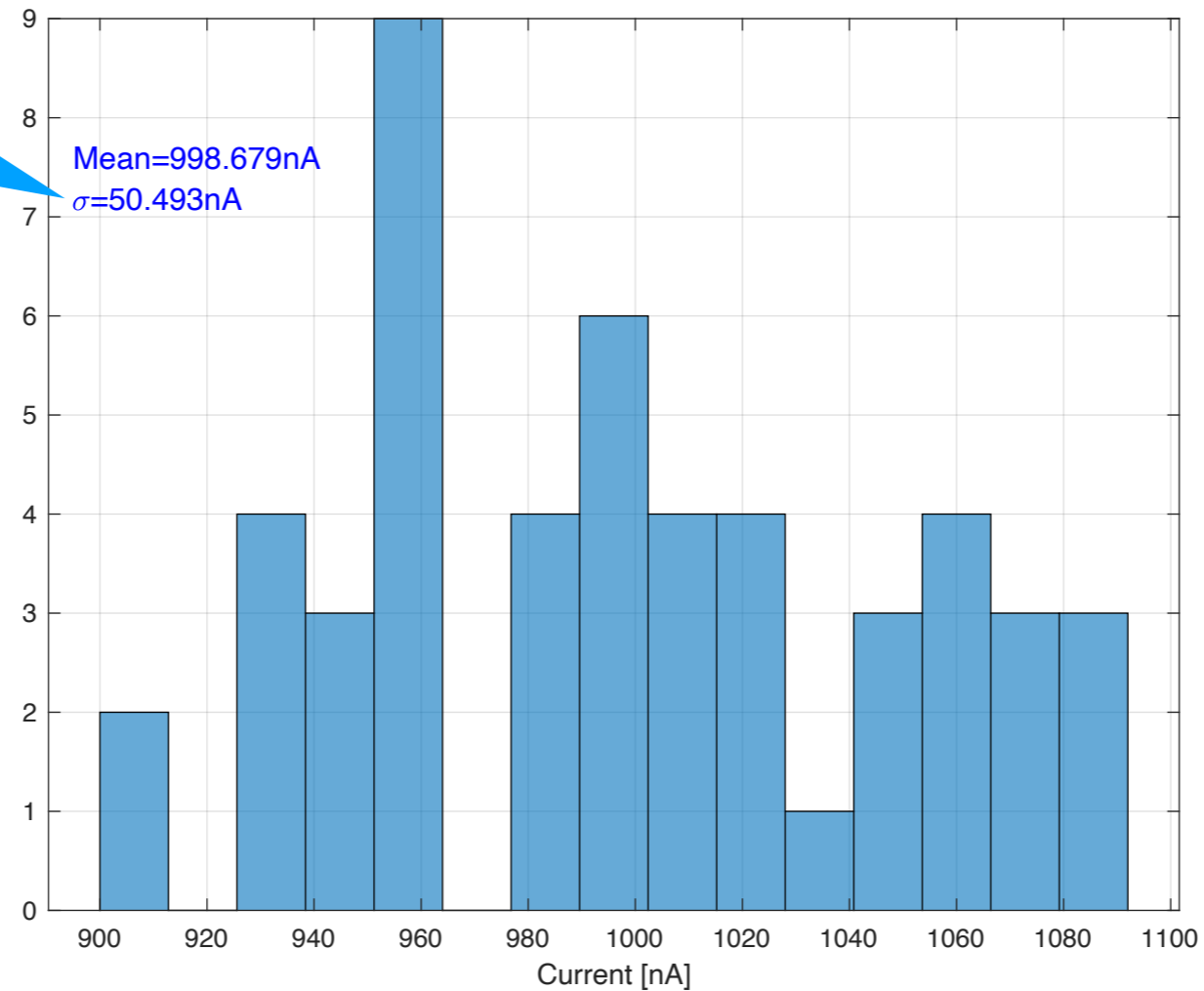
- W=1μm, L=3μm



1.8V LVT PMOS Monte Carlo sim result

- $W=1\mu\text{m}$, $L=3\mu\text{m}$

$$6\sigma = \frac{6 * 50.493\text{nA}}{998.679\text{nA}} = 30.3\%$$



Summary

Bias=1 μ A					
Device	W	L	Vdsat	Vth	6 sigma
1.8V NMOS	1 μ m	5 μ m	~203mV	~539mV	15.2%
	2 μ m	10 μ m	~167mV	~567mV	8.4%
	0.5 μ m	5 μ m	~310mV	~502mV	22.8%
	1 μ m	4 μ m	~198mV	~509mV	19.4%
1.8V LVT NMOS	1 μ m	4 μ m	~160mV	~458mV	26.3%
1.8V PMOS	1 μ m	4 μ m	~327mV	~912mV	13.9%
	2 μ m	2 μ m	~176mV	~962mV	27.5%
1.8V LVT PMOS	1 μ m	3 μ m	~306mV	~435mV	30.3%